FIG. 59 shows a further embodiment of the present invention, in which a resistor R_L' is connected between the collector of the memory cell transistor and the joint of the emitter of the clamping transistor and the series resistor for the SBD. With this construction, also, the degree of freedom in designing a low memory cell potential is increased, and flexible design can be permitted.

FIG. 60 shows a still further embodiment of the present invention, which also ensures flexible designing and increased immunity from soft error.

According to the present invention, by connecting a clamping transistor in parallel with each load in a memory cell of the type in which loads are selectively used under the function of SBDs, it is possible to obtain a large read current of at least several milliamperes even where the series resistor for the SBD has a high resistance, which has an eminent effect on high-speed operation of a high-capacity memory.

As apparent from the foregoing description, the present invention provides transistor constructions which facilitate the adjustment of the width of the base, have a small parasitic capacitance and have the immunity from noise.

Naturally, the present invention is effective also when the p type and the n type are inverted to n type and p type, respectively.

Although the invention has been described in its preferred forms with a certain degree of particularity, it is to be understood that various changes and modifications may be made in the invention without departing from the spirit and scope thereof.

What is claimed is:

1. A semiconductor device comprising:
a semiconductor substrate;
memory cells, each of which comprises first and second inverse-mode bipolar transistors cross-coupled with each other, provided on the semiconductor substrate, and first and second load devices provided on the semiconductor substrate;
word lines for selecting the memory cells, provided on the semiconductor substrate;
bit lines for reading and writing information of the memory cells, provided on the semiconductor substrate; and
coupling devices for electrically coupling the bit lines and memory cells, provided on the semiconductor substrate
wherein:
the first inverse-mode bipolar transistors comprise buried layers,
the second inverse-mode bipolar transistors comprise buried layers,
the first load devices comprise buried layers,
the second load devices comprise buried layers,
the buried layers of the first inverse-mode bipolar transistors are isolated from the buried layers of the first and second load devices,
the buried layers of the second inverse-mode bipolar transistors are isolated from the buried layers of the first and second load devices;
the first inverse-mode bipolar transistors employ the buried layers as emitters, and
the second inverse-mode bipolar transistors employ the buried layers as emitters.

2. A semiconductor device according to claim 1, wherein:
a base of the first inverse-mode bipolar transistor is electrically coupled to a collector of the second inverse-mode bipolar transistor and the second load device,
a base of the second inverse-mode bipolar transistor is electrically coupled to a collector of the first inverse-mode bipolar transistor and the first load device,
emitters of the first and second inverse-mode bipolar transistors are electrically coupled to the word lines, and
the first and second load devices are Schottky barrier diodes.

3. A semiconductor device according to claim 2, further comprising shielding means for shielding the Schottky barrier diodes from noise produced within the semiconductor substrate.

4. A semiconductor device according to claim 1, further comprising shielding means for shielding the first and second load devices from noise produced within the semiconductor substrate.

5. A semiconductor device comprising:
a semiconductor substrate;
memory cells, each of which comprises first and second inverse-mode bipolar transistors cross-coupled with each other, provided on the semiconductor substrate, and first and second load devices provided on the semiconductor substrate;
word lines for selecting the memory cells, provided on the semiconductor substrate;
bit lines for reading and writing information of the memory cells, provided on the semiconductor substrate; and
coupling devices for electrically coupling the bit lines and memory cells, provided on the semiconductor substrate,
wherein:
the first inverse-mode bipolar transistors comprise buried layers,
the second inverse-mode bipolar transistors comprise buried layers;
the coupling devices comprise buried layers,
the buried layers of the first inverse-mode bipolar transistors are isolated from the buried layers of the coupling devices,
the buried layers of the second inverse-mode bipolar transistors are isolated from the buried layers of the coupling devices,
the first inverse-mode bipolar transistors employ the buried layers as emitters, and
the second inverse-mode bipolar transistors employ the buried layers as emitters.

6. A semiconductor device according to claim 5, wherein:
a base of the first inverse-mode bipolar transistor is electrically coupled to a collector of the second inverse-mode bipolar transistor and the second load device,
a base of the second inverse-mode bipolar transistor is electrically coupled to a collector of the first inverse-mode bipolar transistor and the first load device,
emitters of the first and second inverse-mode bipolar transistors are electrically coupled to the word lines, and
the first and second load devices are Schottky barrier diodes.

7. A semiconductor device according to claim 6, further comprising shielding means for shielding the